REMARKS

Claims 3-17 are pending in this application of which claims 3, 4 and 9 are independent. Claims 4-15 and 17 stand allowed. Claims 3 and 16 remain at issue. For the following reasons, the application is deemed to be in a condition for allowance.

Claims 3 and 15 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Motomura (U.S. Patent No. 6,338,108). However, section 102(e) should have been applied, not § 102(b), because the present application was filed after the application for patent by Motomura but before issuance thereof. Nevertheless, the rejection is respectfully traversed.

Claim 16 has been objected to for being dependent upon rejected base claim 3, but would otherwise be allowable if rewritten in independent form. As explained below, claim 3 is in allowable form. Accordingly, this application as currently presented, is in condition for allowance.

In section 3 of the Office Action, the Examiner addresses the teachings of Motomura. The Examiner relies on Fig. 2C and associated description in the background section of Motomura, namely column 2, line 40 through column 3, line 38. Fig. 2C illustrates an example of a connection between packet-type DRAM 1001 and a microprocessor 9 via a packet-type memory bus, having a control section 1012, a unidirectional request bus 1002-3 and a unidirectional response bus 1002-4. Address signals, control signals and data are transferred in packet form. In Motomura, terminal 24 is a control input terminal, terminal 25 is a write data input terminal, and terminal 26 is a data output terminal. The Examiner asserts that both the control terminal 24 and write data input terminal 25 correspond to the claimed input terminals, and terminal 26 corresponds to the claimed output terminal. Hence, at least one output terminal (i.e., data output terminal 26) is different in number from the input terminal(s) (i.e., the control terminal 24 and write data input terminal 25) for receiving the write data. Applicant respectfully disagrees.

The Examiner has mischaracterized claim 1. Claim 1 recites "a plurality of input terminals for receiving write data, a control signal and an address signal," and "at least one output terminal, different in number from the input terminal(s) for receiving the write data, for outputting the read data." It is important to note that the "the input terminal(s) for receiving the write data" does not include the input terminal(s) of the "plurality of input terminals for receiving...a control signal..." In other words, the input terminal(s) for receiving the write data is different in number from the at least one output terminal for outputting read data. In Motomura, there is disclosed only one input terminal for receiving write data and only one output terminal for outputting read data.

In Motomura, the bit width of output data is the same as the bit width of input data, and therefore, the number of output terminals must equal the number of input terminals, contrary to the recitation of claim 1. As described in col. 3, line 50 et seq. in Motomura, the access data length is any of 8 to 256 bytes, but access (write and read) data has a fixed bit length. The data bit length is set by the data length designating data stored in the control register. Data are formed into packets to be transferred, the bus bit width is the same for the data reading path and the data writing path. As such, the data bit width is the same for output data and for input data. It follows that the number of input terminals must be the same as the number of output terminals, given both input data and output data have the same bit width.

Motomura fails to disclose or suggest at least one output terminal, different in number from the input terminal(s) for receiving the write data, for outputting the read data, as claim 1 recites. Supporting Applicant's argument, exemplary Fig. 15 of the present application illustrates an input-width setting circuit 70b that sets the bit width of input circuit 70a according to the input bit width input setting signal IBS. Thus, the terminals receiving the write data may be all of the input data terminals or may be part of the input data terminals. It is important to note that the input

terminals include the data terminals and the control terminals both in Motomura and in the above-described exemplar, but claim 1 refers to the terminals for receiving write data, not the terminals for receiving control signals, by the recitation of "at least one output terminal, different in number from the input terminal(s) for receiving the write data, for outputting the read data." Nowhere does Motomura disclose or suggest that the input terminals "for receiving write data" is different in number from the at least one output terminal "for outputting read data." (*Emphasis added*).

Claim 15 is patentable at least based on the foregoing arguments. For the above reasons, withdrawal of the anticipation rejection of claims 3 and 15 is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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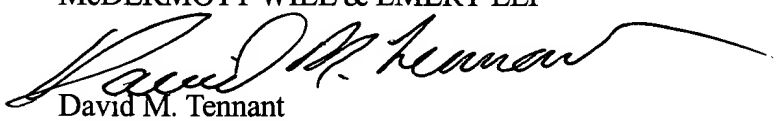

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